Vivekananda College of Engineering & Technology,Puttur
[A Unit of Vivekananda Vidyavardhaka Sangha Puttur ®]
Affiliated to VTU, Belagavi & Approved by AICTE New Delhi

PREPARATORY EXAM

Dept: EC	Sem: **3EC A & B**	Course: **Computer Organization and Architecture**	Course Code: **18EC35**
Date: 26.02.2021	Time: 9:30am-12.30pm	Max Marks: 100	Elective: N
Note: Answer any 5 full questions, choosing one full question from each module.			

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QN		Questions	Marks
		Module1	
1	a	With a neat diagram, explain the basic operational concept of computer.	10
	b	Explain in brief, the key performance parameters that affect the processor performance.	5
	c	Represent 85.125 in IEEE floating point using single precision	5
		OR	
2	a	Illustrate instructions and instruction sequencing with an example.	10
	b	Explain Big-endian and Little-endian assignment.	4
	c	Explain the following with example i)Three address instruction ii)Two address instruction	6
		Module2	
3	a	Discuss following addressing modes with example: i)Immediate ii)Register iii)Direct iv) Indirect v)Index	10
	b	Explain condition codes with example.	6
	c	Explain rotate instruction with example.	4
		OR	
4	a	What are assembler directive? Explain any five assembler directive.	10
	b	Write an assembly language program to add 'n' numbers.	6
	c	With example explain push and pop instruction.	4
		Module3	
5	a	Showing the possible register configuration in I/O interface, explain program controlled input/output	10
	b	Highlight the necessity of Direct Memory Access in a computer system. Also, explain the registers involved in a DMA interface, to illustrate DMA	6
	c	Explain the concept of vectored interrupt.	4
		OR	
6	a	What is an interrupt? With an example illustrate the concept of interrupt.	10

Prepared by: Suhandas HOD

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	b	Explain the following method of handling interrupts from multiple devices i)Daisy chain method ii) Priority structure	10

		Module4	
7	a	Illustrate the internal structure of static memories.	8
	b	With a neat diagram explain virtual memory organization.	8
	c	Briefly explain any two non-volatile memory.	4
		OR	
8	a	With a neat figure explain internal organization of 2M x 8 dynamic memory chip.	10
	b	Describe the working principle of magnetic disk.	6
	c	Write a note on cache memory.	4

		Module5	
9	a	With the neat diagram explain the single bus organization of data path inside a processor.	10
	b	Discuss the organization of hardwired control unit.	5
	c	With diagram explain basic organization of micro-programmed control unit	5
		OR	
10	a	Write down the control sequence for execution of instruction ADD (R3), R1.	10
	b	Explain the three bus organization of the processor and its advantages.	10